What is claimed is:

1. An FIR filter comprising a selection control means for selecting input data, and a multiplying means for multiplying data selected by the selection control means and predetermined filter coefficient, wherein the FIR filter output is derived from the product output of the multiplying means.

2. An FIR filter comprising:

a selection control means, for selecting input data, including a first n-bit shift register (n being natural number for progressively shifting the input data through the successive stage bits, n switching means provided for the outputs of the n stage bits of the shift register, respectively, for on-off controlling the feed-out of the output of these stage bits, and a control means for on-off controlling the n switching means; and

a multiplying means for multiplying data selected by the selection control means and predetermined filter coefficient,

wherein the multiplying means provided for the outputs of the n stage bits of the shift register for multiplying outputs fed out from the corresponding stage bits under "on" control of the switching means by predetermined filter coefficients, respectively, and the FIR filter output being derived from the product outputs of the n multiplying circuits.

3. The FIR filter according to claim 2, wherein:

the control means is constituted by a second n-bit shift register for shifting a ramp-up/-down signal through the successive bit stages under control of a shift clock for the first n-bit shift register; and

the n switch means are each an AND gate for receiving the outputs of the corresponding bit stages of the first and second n-bit shift registers as respective inputs.

4. The FIR filter according to claim 2, wherein:

the control means is a second n-bit shift register for shifting a ramp-up/-down signal on the basis of the shift clock signal of the first n-bit shift register; and

the n switching means are n switches provided for the bit stages of the second n-bit shift register for selectively feeding out the filter coefficient data and zero data on the basis of the outputs of the corresponding bit stages.

5. The FIR filter according to claim 2, wherein the control means is a second n-bit shift register for shifting a ramp-up/-down signal through the successive bit stages under control of a shift clock signal for the first n-bit shift register, the outputs of the bit stages of the first n-bit shift register being reset on the basis of the outputs of the corresponding bit stage of the second n-bit shift register.

6. The FIR filter according to claim 2, which further comprises a means for changing the shift clock frequency of the first n-bit shift registers.

7. The FIR filter according to claim 2, in which the shifting operation of the first and second n-bit shift registers are operated under control of shift clock signals at different frequencies.

8. A ramp-up circuit comprising the FIR filter according to claim 2 which includes an adder circuit for adding together the outputs of the n multiplying circuits, a ramp-up signal being fed to the first n-bit shift register, the ramp-up data being derived from the sum output of the adder circuit.

9. A ramp-down circuit comprising the FIR filter according to claim 2 which includes an adder circuit adding together the outputs of the n multiplying circuit, a ramp-down signal being fed to the first n-bit shift register, ramp-down data being derived from the sum output of the adder circuit.